AMENDMENTS TO THE CLAIMS

1-38. (Canceled)

39. (Currently amended) A method of fabricating a programmable resistance memory element, comprising the steps of:

forming a first ferromagnetic layer having at least one side wall;

forming a second ferromagnetic layer having at least one side wall; and

forming a barrier layer between said first ferromagnetic layer and said second ferromagnetic layer;

wherein said at least one side wall of said first ferromagnetic layer extends laterally beyond said at least one side wall of said second ferromagnetic layer; and

wherein the relative magnetization directions of said first and said second ferromagnetic layers is programmable to set a resistance of said memory element.

40. (Original) A method of claim 39 wherein said at least one side wall of said first ferromagnetic layer extends laterally at least about 10 angstroms beyond said at least one side wall of said second ferromagnetic layer.

41. (Original) A method of claim 40 wherein said at least one side wall of said first ferromagnetic layer extends laterally about 200 angstroms beyond said at least one side wall of said second ferromagnetic layer.

42. (Original) A method of claim 39 wherein said first ferromagnetic layer has a thickness of about 20 angstroms to about 100 angstroms.

43. (Original) A method of claim 42 wherein said first ferromagnetic layer has a thickness of about 20 angstroms to about 50 angstroms.

44. (Original) A method of claim 39 wherein said second ferromagnetic layer has a thickness of about 20 angstroms to about 100 angstroms.

45. (Original) A method of claim 44 wherein said second ferromagnetic layer has a thickness of about 20 angstroms to about 50 angstroms.

46. (Original) A method of claim 39 further comprising the step of forming an antiferromagnetic layer over said second ferromagnetic layer.

47. (Original) A method of claim 46 wherein said antiferromagnetic layer has a thickness of about 70 angstroms to about 150 angstroms

48. (Original) A method of claim 46 wherein said antiferromagnetic layer comprises iridium manganese.

49. (Original) A method of claim 46 further comprising the step of forming a protective layer over said antiferromagnetic layer.

50. (Original) A method of claim 49 further comprising the step of forming an etch mask on said protective layer.

51. (Original) A method of claim 50 further comprising the step of etching the formed layers back beyond said second ferromagnetic layer but before said

first ferromagnetic layer, providing an etched memory element and a side wall for said second ferromagnetic layer.

52. (Original) A method of claim 51 wherein said step of etching ceases at said barrier layer.

53. (Original) A method of claim 51 further comprising the step of forming at least one spacer located over said first ferromagnetic layer and lateral to said second ferromagnetic layer.

54. (Original) A method of claim 53 wherein said at least one spacer comprises a dielectric material.

55. (Original) A method of claim 53 wherein said at least one spacer extends laterally at least about 10 angstroms beyond said side wall of said second ferromagnetic layer.

56. (Original) A method of claim 55 wherein said at least one spacer extends laterally about 200 angstroms beyond said side wall of said second ferromagnetic layer.

57. (Original) A method of claim 53 wherein said step of forming at least one spacer comprises the steps of:

forming a spacer-constituent layer on said etched memory element; and

etching said spacer-constituent element back forming an etched memory element having at least one spacer.

58. (Original) A method of claim 53 further comprising the step of etching said etched memory element having at least one spacer back beyond said first ferromagnetic layer.

59. (Original) A method of claim 39 further comprising the step of forming an antiferromagnetic layer beneath said first ferromagnetic layer.

60. (Original) A method of claim 59 wherein said antiferromagnetic layer has a thickness of about 70 angstroms to about 150 angstroms

61. (Original) A method of claim 59 wherein said antiferromagnetic layer comprises iridium manganese.

62. (Original) A method of claim 59 further comprising the step of forming a protective layer over said antiferromagnetic layer.

63. (Original) A method of claim 62 further comprising the step of forming an etch mask on said protective layer.

64. (Original) A method of claim 63 further comprising the step of etching the formed layers back beyond said second ferromagnetic layer but before said first ferromagnetic layer, providing an etched memory element and side wall for said second ferromagnetic layer.

65. (Original) A method of claim 64 wherein the step of etching ceases at said barrier layer.

66. (Original) A method of claim 64 further comprising the step of forming at least one spacer located over said first ferromagnetic layer and lateral to said second ferromagnetic layer.

67. (Original) A method of claim 66 wherein said at least one spacer comprises a dielectric material.

68. (Original) A method of claim 66 wherein said at least one spacer extends laterally at least about 10 angstroms beyond said side wall of said second ferromagnetic layer.

69. (Original) A method of claim 68 wherein said at least one spacer extends laterally about 200 angstroms beyond said side wall of said second ferromagnetic layer.

70. (Original) A method of claim 66 wherein said step of forming at least one spacer comprises the steps of:

forming a spacer-constituent layer on said etched memory element; and

etching said spacer-constituent element back forming an etched memory element having at least one spacer.

71. (Original) A method of claim 66 further comprising the step of etching said etched memory element having at least one spacer back beyond said first ferromagnetic layer.

72. (New) A method of fabricating a programmable resistance memory element comprising the steps of:

forming a first ferromagnetic layer having at least one side wall;

forming a barrier layer over said first ferromagnetic layer;

forming a second ferromagnetic layer over said barrier layer having at least one side wall; and

forming an antiferromagnetic layer for pinning one of said first and said second ferromagnetic layers;

wherein one of said first and said second ferromagnetic layers extends laterally at least about 10 angstroms beyond said at least one side wall of the other of said first and said second ferromagnetic layers; and

wherein the relative magnetization directions of said first and said second ferromagnetic layers is programmable to set a resistance of said memory element.

73. (New) The method of claim 72, wherein said one of said first and said second ferromagnetic layers extends laterally from about 10 angstroms to about 200 angstroms beyond said at least one side wall of the other of said first and said second ferromagnetic layers.

74. (New) The method of claim 73, wherein said one of said first and said second ferromagnetic layer extends laterally about 200 angstroms beyond said at least one side wall of the other of said first and said second ferromagnetic layers.

75. (New) A method of fabricating a programmable resistance memory element comprising the steps of:

forming a substrate;

forming a seed layer comprising tantalum over said substrate;

forming a first ferromagnetic layer having at least one side wall formed over said seed layer;

forming a barrier layer comprising an aluminum oxide tunnel barrier formed over said first ferromagnetic layer;

forming a second ferromagnetic layer having at least one side wall formed over said barrier layer;

forming an antiferromagnetic layer comprising iridium manganese formed over said second ferromagnetic layer; and

forming a protective layer comprising tantalum formed over said antiferromagnetic layer;

wherein said at least one side wall of said first ferromagnetic layer extends laterally at least about 10 angstroms beyond said at least one side wall of said second ferromagnetic layer; and

wherein the relative magnetization directions of said first and said second ferromagnetic layers is programmable to set a resistance of said memory element.

76. (New) A method of fabricating a programmable resistance memory element comprising the steps of:

forming a substrate;

forming a first seed layer comprising tantalum having at least one side wall formed over said substrate;

forming a second seed layer comprising nickel iron formed over said first seed layer;

forming an antiferromagnetic layer comprising iridium manganese formed over said second seed layer;

forming a first ferromagnetic layer having at least one side wall formed over said antiferromagnetic layer;

forming a barrier layer comprising an aluminum oxide tunnel barrier formed over said first ferromagnetic layer;

forming a second ferromagnetic layer having at least one side wall formed over said barrier layer; and

forming a protective layer comprising tantalum formed over said second ferromagnetic layer;

wherein said at least one side wall of said first ferromagnetic layer extends laterally at least about 10 angstroms beyond said at least one side wall of said second ferromagnetic layer; and

wherein the relative magnetization directions of said first and said second ferromagnetic layers is programmable to set a resistance of said memory element.